FLEXIBLE CASCODE AMPLIFIER CIRCUIT WITH HIGH GAIN FOR FLASH MEMORY CELLS

1. TECHNICAL FIELD

5   The present invention relates generally to the field of semiconductor devices.

More particularly, the present invention relates to semiconductor memory devices.

2. BACKGROUND ART

Memory devices are known in the art for storing data in a wide variety of

electronic devices and applications. A typical flash memory device comprises a

10   number of memory cells. Often, memory cells are arranged in an array format, where

a row of memory cells corresponds to a word line and a column of memory cells

corresponds to a bit line, and where each memory cell defines a binary bit, i.e., either a

zero ("0") bit or a one ("1") bit.

Typically, the state of a memory cell is determined during a read operation by

15   sensing the current drawn by the memory cell. According to one particular

embodiment, the current drawn by a particular memory cell (also referred to as "target

memory cell" or "core memory cell") is ascertained by connecting the drain terminal

of the memory cell to a sensing circuit, where the source terminal of the memory cell

is connected to ground, and the gate of the memory cell is selected. The sensing

20   circuit attempts to detect the current drawn by the memory cell (also referred to as

"target memory cell current" or "core cell current"), and compares the sensed memory

cell current against a reference current. If the sensed memory cell current exceeds the

reference current, the memory cell is considered an erased cell, e.g., corresponding to

a "1" bit. However, if the sensed memory cell current is below the reference current, the memory cell is considered a programmed cell, e.g., corresponding to a "0" bit.

Cascode amplifiers are known in the art for converting current to voltage. Current to voltage conversion is particularly useful when a comparison between a first

5 current, such as that drawn by a target memory cell, and a second current, such as that drawn by a reference memory cell, is required. The reason is that voltage comparators, such as operational amplifiers, for example, are readily available for comparing two voltage values. Accordingly, the conventional approach in comparing two current values involves first converting the current values to voltage values, and

10 then comparing the voltage values using an operational amplifier or other voltage comparator. In this way, during a read operation involving a target memory cell, a conventional cascode amplifier supplies a bit line voltage to the drain of the target memory cell, and generates a sense amp input voltage which corresponds to the current drawn by the target memory cell. Similarly, a sense amp reference voltage can

15 be ascertained corresponding to the current drawn by a reference memory cell, and the sense amp input voltage and the sense amp reference voltage can be compared to determine the state of the target memory cell.

Known cascode amplifiers, however, suffer from a number of problems, which negatively impact the performance of flash memory devices. Typically, conventional

20 cascode amplifiers produce a relatively low DC gain (from the bit line voltage to the sense amp input voltage), particularly at low current, e.g., when a programmed target memory cell draws low current. As a result, the signal generated at the sense amp

input voltage is considerably limited, and, thus, accuracy in identifying the state of the

target memory cell is negatively impacted, and read operations of the flash memory

device are degraded. Furthermore, the bit line voltage supplied to the drain of the

target memory cell achieved by conventional cascode amplifiers have a limited range

5   and, therefore, cannot be flexibly used for various types of memory cells that require a

drain voltage outside of the limited range provided by conventional cascode

amplifiers.

Accordingly, there exists a strong need in the art to overcome deficiencies of

known cascode amplifier circuits, such as those described above, and to provide a

10   flexible cascode amplifier circuit with high gain for flash memory devices.

H1813

SUMMARY

The present invention addresses and resolves the need in the art for a flexible cascode amplifier circuit with high gain for flash memory devices. During a read operation involving a target memory cell, the cascode amplifier circuit is connected to

5   the target memory cell via a bit line, typically by a selection circuit. According to one exemplary embodiment, the cascode amplifier circuit comprises a first intrinsic FET, a second intrinsic FET, a third intrinsic FET, and a fourth FET. The first intrinsic FET has a source connected to the bit line and a drain connected to a first node. The second intrinsic FET has a gate connected to the source of the first intrinsic FET and a

10   source connected to a reference voltage, such as ground. The second intrinsic FET also has a drain connected at a second node to a gate of the first intrinsic FET. The third intrinsic FET has a source connected to the first node and a gate connected to a supply voltage, and further provides a load across the supply voltage and the first node. The fourth FET has a source connected to the second node and a drain

15   connected to the supply voltage, the fourth FET having a gate connected to an input control voltage. With this arrangement, a bit line voltage having a wide range is generated at the source of the first intrinsic FET, and a sense amp input voltage with high gain is generated at the first node.

According to another embodiment of the invention, the second intrinsic FET

20   operates in the saturation region. In one particular embodiment, the second intrinsic FET has a gate width to gate length ratio of approximately 6/0.9. According to another embodiment, the cascode amplifier circuit is activated by first and second

enable transistors. For example, according one particular embodiment, the third intrinsic FET has a drain connected to the supply voltage through a first enable transistor, the fourth FET having a drain connected to the supply voltage through a second enable transistor.

5   Other features and advantages of the present invention will become more readily apparent to those of ordinary skill in the art after reviewing the following detailed description and accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 depicts a circuit diagram of an exemplary cascode amplifier circuit according to one embodiment of the present invention.

Figure 2 depicts a graph illustrating the bit line voltage as a function of the control voltage achieved according to an exemplary cascode amplifier circuit according to one embodiment of the present invention.

Figure 3 depicts a graph illustrating the bit line voltage as a function of the control voltage achieved according to a conventional cascode amplifier circuit.

Figure 4 depicts a graph comparatively illustrating the gain achieved by an exemplary cascode amplifier circuit according to one embodiment of the present invention and the gain achieved by a conventional cascode amplifier circuit.

H1813

DETAILED DESCRIPTION OF THE INVENTION

The present invention is directed to a flexible cascode amplifier circuit with

high gain for flash memory devices. The following description contains specific

information pertaining to the implementation of the present invention. One skilled in

5   the art will recognize that the present invention may be implemented in a manner

different from that specifically discussed in the present application. Moreover, some

of the specific details of the invention are not discussed in order not to obscure the

invention.

The drawings in the present application and their accompanying detailed

10   description are directed to merely exemplary embodiments of the invention. To

maintain brevity, other embodiments of the present invention are not specifically

described in the present application and are not specifically illustrated by the present

drawings.

Referring to Figure 1, there is shown a circuit diagram of exemplary cascode

15   amplifier circuit 102 according to one embodiment of the present invention. Cascode

amplifier circuit 102 may be part of larger circuit arrangement 100 which itself may be

part of a flash memory device.

In Figure 1, cascode amplifier circuit 102 supplies bit line voltage ("DATAB")

120 to the drain of target memory cell 112 via bit line 116 during a read operation

20   involving target memory cell 112, and generates sense amp input voltage ("SAIN")

122 corresponding to target memory cell current 118 (also referred to as "core cell

current 118" and "Icore 118") drawn by target memory cell 112 during the read

operation. As discussed below, cascode amplifier circuit 102 provides higher DC gain at SAIN 122, resulting in significantly improved read operations involving target memory cell 112. Also discussed below, cascode amplifier circuit 102 provides a wider voltage range via DATAB 120, thereby allowing cascode amplifier circuit 102

5   to be flexibly used for a variety of flash memory cells, including memory cells capable of storing a single bit and memory cells capable of storing two independent bits in separate locations within the memory cell, such as Advanced Micro Devices, Inc. (AMD) MirrorBit™ memory devices, for example.

As shown in Figure 1, cascode amplifier circuit 102 comprises FETs 104, 106,

10   108, and 110, where the source of FET 104 at node 120 is connected to the drain of target memory cell 112, typically by a selection circuit (not shown), through bit line 116 during a read operation involving target memory cell 112. During the read operation, the source of target memory cell 112 is also connected to a reference voltage, such as ground 130, and the gate of target memory cell 112 is selected to turn

15   on target memory cell 112, which draws Icore 118 via bit line 116. PFET 124 and PFET 126 operate as enable transistors to switch on cascode amplifier circuit 102 during a read operation involving target memory cell 112. More specifically, PFET 124 is enabled to connect supply voltage ("VCC") 128 to the drain of PFET 108, PFET 126 is enabled to connect VCC 128 to the drain of PFET 110.

20   In accordance with one embodiment of the invention, FETs 104, 106 and 108 comprise intrinsic NFETs each having a threshold voltage ("Vt") in the range of approximately 0.3 to 0.5 V, and FET 110 comprises an NFET having a Vt in the range

H1813

of approximately 0.7 to 1 V. By way of example, FET 104 has a gate width to length

ratio ("W/L") of approximately 45/0.9, FET 106 has a W/L of approximately 6/0.9,

FET 108 has a W/L of approximately 4/8, and FET 110 has a W/L of approximately

6/1. As shown in Figure 1, the source of FET 104 is connected to node 120 and a

5   drain connected to node 122. FET 106 has a gate connected to the source of FET 104

at node 120, and a drain connected to a gate of FET 104 at node 123. FET 106 further

has a source connected to a reference voltage, such as ground 130. FET 108 has a gate

connected to VCC 128, a drain connected to VCC 128 through enable PFET 124, and

a source connected to node 122. FET 110 has a drain connected to VCC 128 through

10   enable PFET 126 and a source coupled to node 123. Control voltage ("DCNT") 132 is

supplied to the gate of FET 110.

       In cascode amplifier circuit 102, FET 104 operates as a primary cascode

transistor, FETs 106 and 110 operate as a negative feedback to FET 104 for stabilizing

DATAB 120, and FET 108 operates as a load a load across VCC 128 and the drain of

15   FET 104. With this arrangement, cascode amplifier circuit 102 generates DATAB

120, which has a lower operating bound and a wider range to accommodate numerous

memory cell types. For example, with reference to Figure 2, graph 200 illustrates

DATAB 120 and current 114 drawn by FET 106 as a function of DCNT 132 sweeping

from 5V to 0V, as achieved by cascode amplifier circuit 102. In Figure 2, DATAB

20   curve 202 corresponds to DATAB 120, current curve 204 corresponds to current 114

drawn by FET 106 when cascode amplifier circuit 102 is activated, and DCNT curve

206 corresponds to DCNT 132 supplied to the gate of FET 110. As shown in graph

200, when current curve 204 approaches the lower bound of approximately 4 micro

Amps (μA) at point 208, cascode amplifier circuit 102 is operating and generates

DATAB 120 of approximately 0.5V (corresponding to DATAB curve 202 at point

210). Thus, with DCNT 132 of approximately 2.5V (corresponding to DCNT curve

5   206 at point 212), cascode amplifier circuit 102 is operating, and DATAB 120 has a

voltage of approximately 0.5V, which is suitable for use with target memory cell 112

capable of storing a single bit. Continuing with graph 200, with DCNT 132 of

approximately 5V (corresponding to DCNT curve 206 at point 216), DATAB 120 has

a voltage of approximately 1.5V (corresponding to DATAB curve 202 at point 214),

10   which is suitable for use with target memory cell 112 capable of storing two binary

bits. As illustrated by the above examples, due to the particular arrangement of

cascode amplifier circuit 102, the flexible and wide voltage range for DATAB 120

achieved by cascode amplifier circuit 102 allows cascode amplifier circuit 102 to be

used with a wide variety of memory cells.

15   In contrast, conventional cascode amplifier circuits have a limited bit line

voltage range. For example, with reference to Figure 3, graph 300 illustrates the

DATAB voltage as a function of the DCNT voltage input achieved by a conventional

cascode amplifier circuit. In Figure 3, DATAB curve 302 corresponds to the bit line

voltage supplied to a target memory cell, current curve 304 corresponds to the current

20   drawn by a conventional transistor that replaces FET 106 in Figure 1, and DCNT

curve 306 corresponds to the control current voltage supplied to the conventional

cascode amplifier circuit. As shown in graph 300, when current curve 304 approaches

the lower bound of approximately 4 μA at point 308, the conventional cascode amplifier circuit generates a bit line voltage of approximately 0.9V (corresponding to DATAB curve 302 at point 310). Continuing with graph 300, the upper bound of DATAB curve 302 at point 312 corresponds to a bit line voltage of approximately

5   1.8V, and thus, the bit line voltage range achieved by the conventional cascode amplifier circuit has a significantly limited range of approximately 0.9V to 1.8V, which severely limits the flexibility of such conventional cascode amplifier circuits to be used with a wide variety of memory cells.

Continuing with Figure 1, cascode amplifier circuit 102 generates SAIN 122

10   corresponding to Icore 118 drawn by target memory cell 112 during a read operation involving target memory cell 112. Due to the particular arrangement of cascode amplifier circuit 102, a significantly higher DC gain is achieved at SAIN 122, while achieving a lower operating voltage at DATAB 120 as discussed above. High DC gain at SAIN 122 is achieved due to the low Vt of FET 106 and due to the large size

15   (W/L) of FET. Thus, even at a low voltage of approximately 0.5V at DATAB 120, which is supplied to the gate of FET 106, FET 106 is capable of operating in the saturation region, and current through FET 106 and FET 110 will not be shut off. Thus, cascode amplifier circuit 102 continues to operate, generating DATAB 120 and SAIN 122. As a benefit, high DC gain 122 is achieved at SAIN 122. With reference

20   to Figure 4, graph 400 illustrates the curves 402 and 404, which correspond respectively the gain achieved by cascode amplifier circuit 102 and a conventional cascode amplifier circuit, where the vertical axis defines SAIN voltage and the

horizontal axis defines the current through the target memory cell, i.e., core cell current. In graph 400, curve 402 corresponds to the gain achieved by cascode amplifier circuit 102 of Figure 1 and curve 404 corresponds to the gain achieved by a conventional cascode amplifier circuit. As shown in graph 400, curve 402 has

5   significantly steeper slope (corresponding to higher gain) over curve 404, particularly at low current. For example, at point 406, curve 402 has a gain of approximately 0.042 V/µA in comparison to curve 404, which has a gain of approximately 0.03 V/µA at point 408.

In sum, cascode amplifier circuit 102 provides increased gain at SAIN 122,

10   which improves the accuracy of read operations involving target memory cell 112, thereby improving the reliability of the flash memory device. Furthermore, due to the particular arrangement of cascode amplifier circuit 102, a wide voltage range for DATAB 120 is achieved, which allows cascode amplifier circuit 102 to be used with a variety of memory cells.

15   From the above description of exemplary embodiments of the invention it is manifest that various techniques can be used for implementing the concepts of the present invention without departing from its scope. Moreover, while the invention has been described with specific reference to certain embodiments, a person of ordinary skill in the art would recognize that changes could be made in form and detail without

20   departing from the spirit and the scope of the invention. For example, the particular operating voltages or voltage ranges referred to in the present application can be modified without departing from the scope of the present invention. The described

exemplary embodiments are to be considered in all respects as illustrative and not

restrictive. It should also be understood that the invention is not limited to the

particular exemplary embodiments described herein, but is capable of many

rearrangements, modifications, and substitutions without departing from the scope of

5   the invention.

Thus, a flexible cascode amplifier circuit with high gain for flash memory

devices has been described.

H1813